

Complex logic Gates:

Complex logic gates are

1) AND-OR-INVERT (AOI) gates

2) OR-AND-INVERT (OAI) gates

These gates are broadly used for realization of complex boolean functions in a single stage.

These gates can be realized very effectively using CMOS technology.

The total number of transistor gates required for the realization of a complex boolean function using complex logic gates [AOI or OAI gates] are very less compared to the realization of same boolean function using NAND gates or NOR gates.

For instance, we need 8 transistors to realize the boolean function $y = \overline{(A \cdot B)} + \overline{(C \cdot D)}$ using AOI or OAI gates. whereas, we need 20 transistors for realization of same boolean function using

NAND or NOR gates.

Due to less number of transistors, the complex logic gates occupy small area, consume less power, speed is high and the fabrication cost is low.

Complex logic gates are especially used to execute complex functions with quite low logical efforts.

Switch logic:-



Figure shows a MOS transistor switch built by connecting n-type and p-type transistors in parallel. The switch transmits logic 0 and logic 1 equally well from source to drain.

so it is called a transmission gate. When V_{DD} or V_{SS} is given at the drain, one gets V_{DD} or V_{SS} at the source. However, it requires two similar transistors and their accompanying bias. It needs both true and complement form of the gate signal.

An alternative is the n-type switch, which is a solitary n-type transistor. It needs only one transistor and one gate signal.

It transmits logic '0' well, but when V_{DD} is applied to the drain, the voltage at source is $V_{DD} - V_{th}$. When switch logic drives gate logic, n-type switches can cause electrical problems. An n-type switch driving a complementary gate causes the complementary gate to run slower. When the switch input is 1, when a lower gate voltage is applied, the complementary pull-down gates will not suck the current fastly off the output capacitance due to

weak n-type pull-down current.

When the n-type switch drives a Pseudo NMOS gate, hazard might rise. A pseudo-NMOS gate ratioded transistor relies on logic 0 and logic 1 inputs to occur within a prescribed voltage range.

If the n-type switch doesn't turn on, the pseudo-NMOS pull down strongly enough. The pull down may not divert sufficient current from the pull up to force the output to logic 0, even if we wait forever. Ratioded logic driven by n-type switches must be designed to yield valid outputs for both polarities of input.

Alternate Gate Circuits:

The six alternating gate circuits are;

- 1) CMOS static logic
- 2) CMOS transmission gate

- 3) Tri-state gate
- 4) Pass transistor logic
- 5) Dynamic CMOS logic
- 6) Domino CMOS logic

Domino CMOS Logic

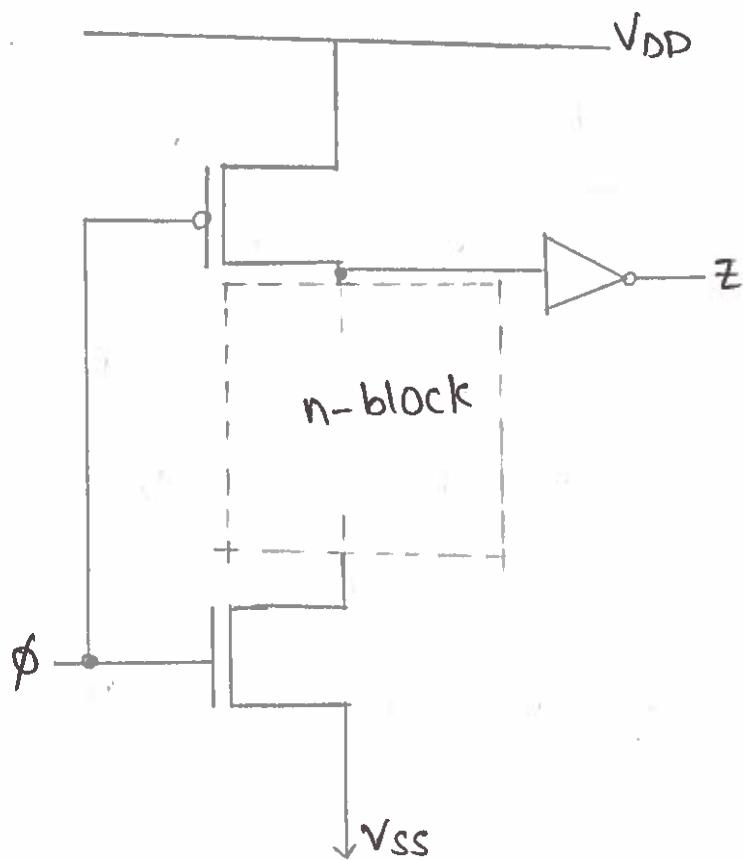


Figure shows an extension to the dynamic CMOS logic referred as CMOS domino logic. The cascading of logic structures using only a single phase clock is allowed by CMOS

domino logic. In each logic gate, this logic requires a static CMOS buffer.

With the help of following points, we can use the above type of logic in different applications. They are,

- 1) As compared to the conventional CMOS logic, these logic structures have smaller areas.
- 2) Higher operating speeds are possible as the value of parasitic capacitances is small.
- 3) Each gate in domino logic can make only one transition i.e., '1' to '0'. Thus, the operation is free to glitches.
- 4) The presence of inverting buffer yields only non-inverting structures in domino logic.
- 5) Even though charge distribution may be a problem, it must be considered.

Time Delays:-

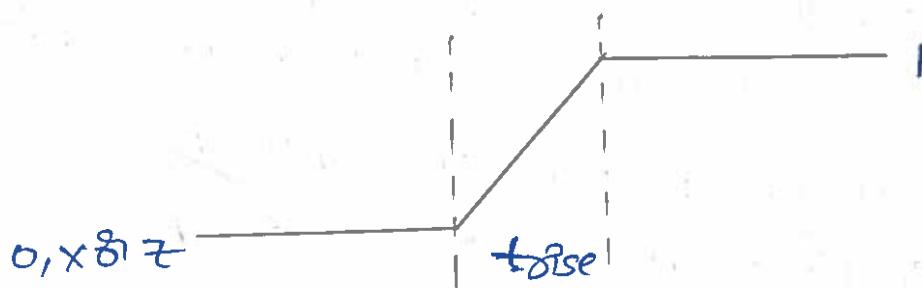
Delay in VLSI circuit is defined as the time required for a digital signal to propagate from inputs to the output

Various Time Delays:-

There are 3 types of time delays in gate level modelling namely,

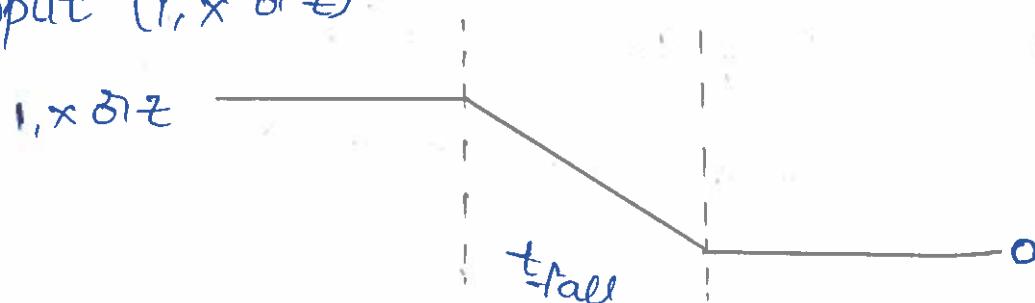
i) Rise Delay (t_{rise})

Rise delay associates the output (1) and input ($0, x, \delta t, z$)



ii) Fall Delay (t_{fall})

Fall delay associates the output (0) and input (1, $x, \delta t, z$)



(iii) Turn-off Delay (t_{off}):

Turn-off delay associates the output (high impedance state (Z)) and input (0 or $1, X$). The specifications of two delays refers to rise and fall delays, and the minimum of these two delays in the turn-off delay. The default value is zero, if no delay is specified.

Driving Large capacitive Loads:-

problems of Driving Large capacitive Loads:-

The problem of driving large capacitive loads comes into the effect, when the signals start propagating from on chip to off chip destinations. It is a result of the off chip load capacitance (C_L) value, which is many times greater than the on chip gate to channel capacitance values ($\square c_g$). Usually,

$$C_L \geq 10^4 \square c_g$$

Because of the large C_L values extremely long delays occur. To

To prevent these extremely long delays, the signals should be driven via low resistances.

Method of using cascaded inverters as

drivers:-

One of the methods to drive such large capacitive loads is by using cascaded inverters as drivers.

The inverters used to drive large capacitive loads should have low pull-up resistance $Z_{P.M}$ and low pull-down resistances $Z_{P.D}$.

In MOS circuits, lower values of $Z_{P.M}$ and $Z_{P.D}$ relates to a lower ϕ value of length to width ratio (i.e., $L:W$). Thus to decrease the resistance value, the channels should be made very wide and in effect, a larger area is occupied by the inverters and the necessity is met. Length (L) cannot be decreased below the minimum feature size.

Hence, the gate region area $L \times W$ becomes more important and a larger capacitance

exists at the input.

In order to overcome this drawback, if cascaded inverters are to be used, the arrangement of these inverters should be such that each one of the inverters is larger than its preceding one by a width factor of f as shown in the figure.

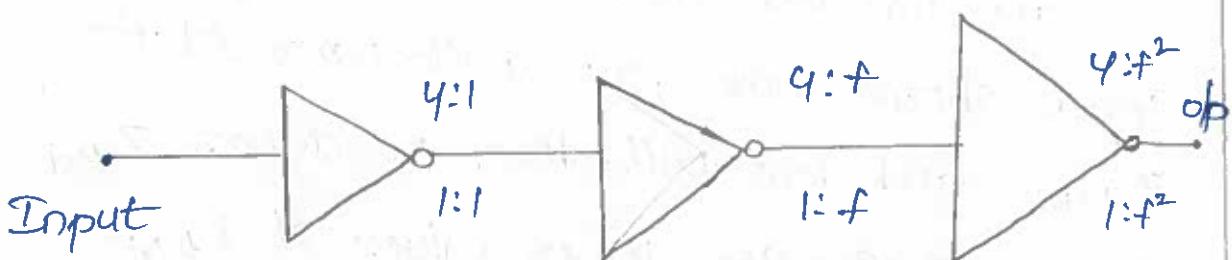


Figure: Cascaded Inverter Driver

As the width factor increases, the capacitive load existing at the inverter input stage and the area occupied too stages. The number of stages (N) to be cascaded to drive a specific value of C_L is decided by the rate at which the channel width increases. The best solution for this is achieved as follows.

with higher values of f , the value of N decreases but the delay per stage increases for 4:1 NMOS inverters.

$$\text{Delay per stage} = f_t \{f_t \Delta V_{in}\}$$

$$= 4f_t \{\Delta V_{in}\}$$

where, ΔV_{in} - Transition of V_{in} from logic 0 to logic 1 and

ΔV_{in} - Transition of V_{in} from logic 1 to logic 0

\therefore Total delay per NMOS pair

$$= f_t + \Delta f_t$$

$$= 5f_t$$

Similarly, total delay per CMOS pair = $7f_t$

In order to make the choice of f and N to be interdependent let

$$y = \frac{C_L}{C_Q} = f^N$$

Applying natural logarithm on both sides,

$$\ln(y) = \ln(f^N) = N \ln(f)$$

$$\Rightarrow N = \frac{\ln(y)}{\ln(f)}$$

\therefore for even N :

$$\begin{aligned}
 \text{Total delay} &= \frac{N}{2} \times 5 \text{ ft} \\
 &= 2.5 N \text{ ft } \{ \text{for NMOS} \} \\
 &= \frac{N}{2} \times 7 \text{ ft} \\
 &= 3.5 N \text{ ft } \{ \text{for CMOS} \}
 \end{aligned}$$

Hence, in either of the cases we have,

$$\text{total delay} \propto N \text{ ft} = \frac{\ln(y)}{\ln(e)} \text{ ft}$$

Therefore, it can be seen that in either of the cases, the total delay is minimized

At $f = e$

$$N = \frac{\ln(y)}{\ln(e)} = \frac{\ln(y)}{e} = \ln(y)$$

For Even values of N :

overall delay time,

$$\begin{aligned}
 t_d &= 2.5 e N \text{ ft } \{ \text{for NMOS} \} \\
 &= 3.5 e N \text{ ft } \{ \text{for CMOS} \}
 \end{aligned}$$

For odd values of N :

for ΔV_{in}

$$\begin{aligned}
 t_d &= [2.5(N-1) + 1] e \text{ ft } \{ \text{for NMOS} \} \\
 &= [3.5(N-1) + 2] e \text{ ft } \{ \text{for CMOS} \}
 \end{aligned}$$

for ∇V_{in}

$$t_d = [2.5(N-1) + 4] e \text{ ft } \{ \text{for NMOS} \}$$

$$= [3.5(N-1) + 5] e^{\pi} \{ \text{for CMOS} \}$$

Wiring capacitance:-

A capacitance which is not concentrated within a capacitor is referred as wiring capacitance.

The various sources of capacitance that contribute to the overall wiring capacitance are

- fringing fields, inter layer capacitances,
- peripheral capacitance.

(i) Fringing Fields

If the accurate prediction of performance is required then the capacitance due to fringing fields (C_f) must be considered. If forms a major part in the overall wiring capacitance. For fine line metallization, the value of V_f can be in the orders of area capacitance.

C_f is given by,

$$C_f = \epsilon_{SiO_2} \epsilon_0 l x \left[\frac{\pi}{\ln \left\{ 1 + \frac{2d}{t} \left(1 + \sqrt{1 + \frac{t}{d}} \right) \right\}} \right]$$

$$= C_W - C_{area}$$

Where, C_W = overall wiring capacitance

C_{area} = Area capacitance

l = Length of the wire

t = Thickness of the wire

d = Wire to substrate separation

(ii) Inter Layer Capacitances:-

From the definition of capacitance itself, it can be said that, there exists a effect capacitance between the layers due to parallel plate effects. Quite obviously, this capacitance will depend upon the layout i.e., whether the layers come in contact or not. By the knowledge of these capacitances, the accuracy of circuit modelling and delay calculations will be improved. It can be readily calculated for regular structures.

iii) Peripherical capacitance:

The source and drain ϕ -diffusion regions forms junctions with the n -substrate (or well) at well defined and uniform depths. Similarly the source and drain n -diffusion regions forms ϕ junctions with the p -substrate at well defined and uniform depths. Hence, for diffusion regions each diode thus formed will associate a peripherical or side-wall capacitance, with it. As a whole the peripherical capacitance, C_p will be in the order of $\text{pF}/\text{unit length}$.

So, its value will be greater than C_{area} of the diffusion region to substrate.

C_p increases with reduction in source & drain area. Total diffusion capacitance is given by,

$$C_{diff} = C_{area} + C_p$$

However, as the n and p -active regions are formed by impure implants at the

surface of the switch in case of orbit processes, they have negligible depth. Hence, C_p is quite negligible in them.

Fan-in and Fan-out:-

Fan-in and Fan-out characteristics of CMOS technologies are shown in figures (1) & (2) respectively.

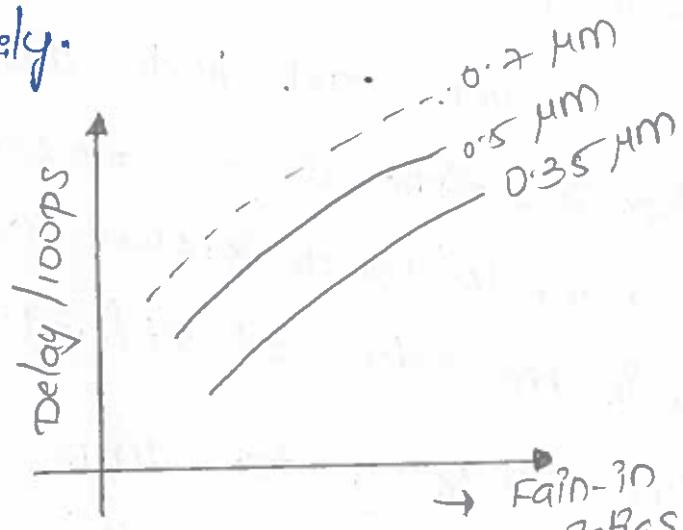


Fig (1) Fan-in characteristics

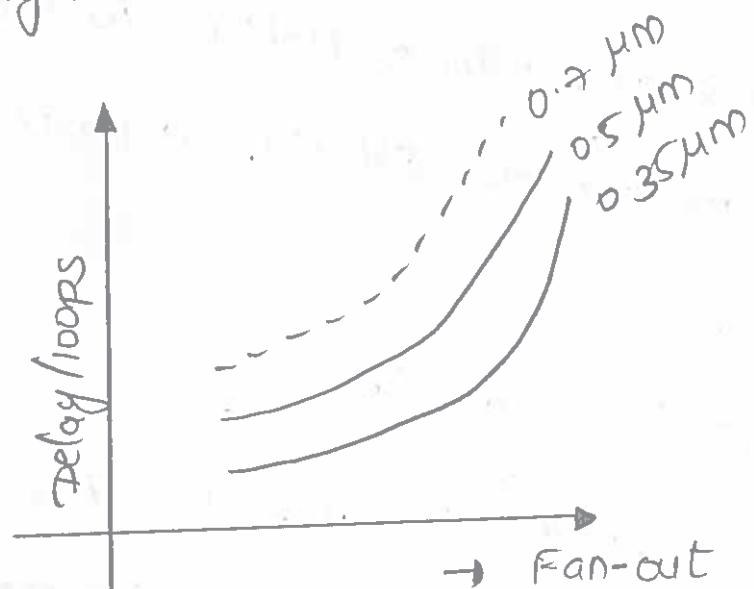


Fig (2) Fan-out characteristics

choice of Layers:

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The following are the constraints which must be considered for the proper choice of layers.

1. Except for very small distances, polysilicon should not be used for routing V_{DD} and V_{SS} (or GND). Long lengths should be used only after careful consideration. This constraint is due to the fact that the polysilicon layer has relatively higher value of R_s .
2. V_{DD} and GND (or V_{SS}) must be distributed only on metal layers. Of course, they can be separated from metals for duck under especially on the diffusion layer when they are absolutely necessary. This constraint is also due to the consideration of R_s value. The capacitive effects will also impose certain restriction in the choice of layers.
3. They must be carefully considered especially where fast signal lines are required &

Fan-in is the number of inputs to an electronic logic gate and fan-out is the number of gates and the length of metal tracks connected to the output of a logic gate. These two factors decide the speed of a logical circuit. (Figure (1)) and (2) Illustrate the delay associated with fan-in and fan-out for $0.7 \mu m$ and $0.35 \mu m$ technologies respectively.

From figure (1), it can be seen that the number of inputs to gate is directly proportional to the delay of the gate. As the number of inputs to a gate increases, it experiences a constant increase in its delay. However, from figure (2) it can be seen that gate experiences a rapid and exponential increase in the delay when the load driven by the gate at the output increases. Hence, as fan-out increases the gate delay increases considerably.

(P)

especially in relation to signals on wiring which has relatively higher values of R_s . Also, the diffusion areas have higher values of capacitance to substrate and are harder to drive. In certain architectures, the problem due to charge sharing must also be carefully considered. over small equipotential regions, the signal on a wire can be treated as being identical at all points. Within each region, the propagation delay of the signal will be comparably smaller than the gate delays and signal delays caused in a system connected by wires.

